USER MANUAL

HVS/UM9704

Version 2.1

Philips
Semiconductors

PHILIPS

REVISION HISTORY

Version	Remarks
0.1	DRAFT; 14.08.96
0.2	Update IIC REGs 24,25; 20.08.96
0.3	Update REG7: ENA_HWE_ROUGH; 21.08.96
1.0	First Release; refers to BESIC-SW from V0.34 until V1.0; 31.10.96 (This UM describes the iic interface of the BESIC for a single memory concept or a PROZONIC concept. The µC ROM of the first BESIC samples contain this interface. MELZONIC control (SAA4991) is not possible via the iic interface described in this document)
2.0	Second Release; refers to BESIC-SW starting with V2.0; 28.02.97 This document describes a new iic interface of the BESIC including the MELZONIC control in addition to the features described in the first release document. An external µC ROM of the first BESIC samples will contain this new iic interface. A new BESIC version, which will be developed, contains the new interface.
2.1	HVS/UM9704, 12.12.97, update of UM9701 V2.0

USER MANUAL

HVS/UM9704
I²C-bus Register Specification for the SAA 4977 V1B

Report No.: HVS/UM9704

Keywords

BESIC
Memory Controller
I²C-Bus
PROZONIC
MELZONIC

Date: 12th of december, 1997

Preface

The specification describes the I²C-bus register interface of an IPQ slave microcontroller (80C51 core), which is a part of the BESIC (SAA 4977). The described interface refers to a BESIC software version which is not implemented in the first BESIC samples. (see Revision History). This interface will replace the old one in future.

The BESIC is a videoprocessing IC providing analog interfacing, video enhancing features, memory controlling and the embedded 80C51 microprocessor core. The slave IPQ µC is used as an interpreter between a main (master) µC and the Datapath Control in BESIC as well as the direct control of the internal memory controller , in case of a two field memory concept, also the PROZONIC (SAA4990; external) or MELZONIC (SAA4991;external).

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1. Introduction

The UM9701 V2.1 describes the IIC interface of the SAA 4977 V1B. The software of this evaluation samples is not completed to support all the possible functions as described in AN97057 and AN 97071. It mainly supports the Melzonic concept. The single field concept runs if the Prozonic concept is chosen in the software. IIC register 37 cannot be controlled if the Prozonic option is set.

The compression modes might show some data failures in the luminance signal. This problem can be eliminated if the supply voltage of BESIC is reduced to 4.2V. For VCR sources problems with the picture stability can occur. The above mentioned restrictions are solved in the next version of the SAA 4977 .

The IIC interface of the final SAA 4977 is described in the document HVS/CR9705.

1.1 Definitions, Acronyms and Abbreviations

HEX	Hexadecimal
HOST interface	BESIC Interface towards 8051 microprocessor core
IPQCS	Improved Picture Quality Control Software
IPQ µC	Improved Picture Quality slave microcontroller
LFR	Line Flicker Reduction by median filtering
MELZONIC	Motion Estimation/compensation, Line flicker reduction, ZOom and Noise reduction IC
MPIP	Multi picture in picture with external PIP processor
NR	Noise reduction (adaptive)
PROZONIC	Progressive Scan, Zoom and Noise Reduction IC

1.2 References

[1] Philips Semiconductors Software Creation Process V1.0; Wilko van Asseldonk, Marc de Smet; April 9th, 1996

[2] Tentative Device Specification for BESIC; 06.08.96; A. Kannengiesser

[3] Tentative Device Specification Control Part BESIC; 24.06.96; G. Stäcker, H. Waterholter

[4] 80C51 microcontroller order form

[5] 80C51 microcontroller Core Specification V1.2; 22.02.96; P. Klapproth

[6] Datapath Control Register; 13.08.96; A. Kannengiesser

[7] Application Note, MK8 Module, AN97057; H. Waterholter

[8] Application Note, MK9 Module, AN97071, H. Waterholter

2. General

The IPQ µC reads register bytes via the I²C-bus from the master µC and sends itself 1 status byte plus following read registers whenever addressed with R/W = 1. The I²C register bytes received are written into the µCs RAM.

3. I²C-bus interface

3.1 Definition of the interface

The interface of the IPQ µC is realized with a hardware I²C-bus.

The slave address of the IPQ µC is 68h:

Slave address = 0 1 1 0 1 0 0 R/W.

The IPQ µC can either act as a slave receiver or a slave transmitter. In the slave receiver mode the IPQ µC reads I²C register data bytes from the main controller which then acts as a master transmitter. In the slave transmitter mode the IPQ µC sends status information to the main µC which works as a master receiver reading the byte information.

3.2 Sending data to the IPQ µC

3.2.1 I²C transmission protocol

The transmission protocol has the following format:

Start	Slave address 68h	Ack	Subad-dress	Ack	REG1	Ack	.....	Ack	REGx	Ack	Stop

After having addressed the IPQ µC with its slave address the master µC transmits the subaddress plus following register bytes over the I²C-bus. The number of register bytes which are transmitted after the transmission of the subaddress is free choosable. It is possible to transmit just one single register byte after having sent the slaveaddress plus subaddress (3 bytes package).

The IPQ µC acknowledges always all register bytes independent of their contents. If the master µC transmits more than the maximum number of register bytes, the slave µC will acknowledge the following bytes, but will not store them in the internal RAM.

Subaddresses starting from 28h onwards indicate, that datapath control registers are to be serviced.

3.2.2 I²C register tables

[Default hex values in brackets]

Table 1: I²C-Register REG1 (FREQUENCY SELECT): Subaddress 00 hex [00]

Bit	Name	Function
0	reserved	to be cleared
1	reserved	to be cleared
2	G_MODE	0: normal mode 1: generator mode on
3	reserved	to be cleared
4	AFF	acquisition field frequency (50/60 Hz): 0 = 50 Hz, 1 = 60 Hz
5	reserved	
6	reserved	
7	INIT	initialize the SAA4977 and MELZONIC (if applied): 0 = off, 1 = on

Table 2: I²C-Register REG2 (FIELD CONTROL); Subaddress 01 hex [01]

Bit	Name	Function
0	LFR	line flicker reduction mode: 0 = off (AABB mode), 1 = on (AA*B*B, ABAB raster)
1		to be cleared
2	reserved	
3	reserved	
4	MOVIE	Forced Movie mode (ABAB raster) 0: off 1: on
5	PHASE	Forced Phase Flag to be set in combination with CINE 0: normal mode 1: 180 deg. phase shift (BCBC)

Table 2: I²C-Register REG2 (FIELD CONTROL); Subaddress 01 hex [01]

Bit	Name	Function
6	AUTO_MOVIE	0: normal mode 1: automatic movie mode activated. In case of a detected movie source, the field processing will switch to cine(movie) mode and the correct movie phase will be processed (MOVIE, PHASE_FLAG are readable via STATUS register)
7	STP	still picture mode 0: off 1: on (one field out of AABB, full frame median filtered out of LFR)

Table 3: I²C-Register REG3 (VZOOM): Subaddress 02 hex [10]

Bit	Name	Function
0	VZOOM_0	Vertival zoom bit 0
1	VZOOM_1	Vertical zoom bit 1
2	VZOOM_2	Vertical zoom bit 2
3	VZOOM_3	Vertical zoom bit 3

Table 3: I²C-Register REG3 (VZOOM): Subaddress 02 hex [10]

Bit	Name	Function				
		V3	V2	V1	V0	Conversion factor
		0	0	0	0	1,1
		0	0	0	1	reserved
		0	0	1	0	1,25
		0	0	1	1	reserved
		0	1	0	0	1,33
		0	1	0	1	reserved
		0	1	1	0	1,5
		0	1	1	1	reserved
		1	0	0	1	2
		1	0	1	0	reserved
		1	0	1	1	reserved
		1	1	0	0	reserved
		1	1	0	1	reserved
		1	1	1	0	reserved
		1	1	1	1	reserved
4	NATURAL_MOTION	0: Natural Motion off 1: Natural Motion aktiv				
5		to be cleared				
6	SAT_MODE	Satellite Mode (removes wiping dots) 0: off (LFR, AABB, AUTO_MOVIE or CINE mode active) 1: on (LFR, AABB, AUTO_MOVIE and CINE not active)				
7	VZOOM	0: Vertical Zoom mode not active 1: Vertical Zoom mode active				

Table 4: I²C-Register REG4 (External Multi PIP): Subaddress 03 hex [00]

Bit	Name	Function
0	POS0	PIP position bit 0
1	POS1	PIP position bit 1
2	POS2	PIP position bit 2
3	POS3	PIP position bit 3
4		to be cleared
5	NPIP	number of PIP's: 0 = 3x3 PIP's, 1 = 4x3 PIP's
6	MPIP	External Multi-PIP: 0 = off, 1 = on
7	SPIP	NTSC PIP: 0 = 50 Hz PIP, 1 = 60 Hz PIP

Table 5: I²C-Register REG5 (NR, SCREEN FADE): Subaddress 04 hex [02]

Bit	Name	Function		
0	NR0	noise reduction bit 0		
1	NR1	noise reduction bit 1		
		NR1	NR0	noise reduction
		0	0	off
		0	1	low
		1	0	middle
		1	1	high
2	SPS0	split screen bit 0		
3	SPS1	split screen bit 1		
		SPS1	SPS0	split screen
		0	X	off
		1	0	horizontal
		1	1	vertical
4	SCF0	screen fade bit 0		

Table 5: I²C-Register REG5 (NR, SCREEN FADE): Subaddress 04 hex [02]

Bit	Name	Function		
5	SCF1	screen fade bit 1		
		SCF1	SCF0	screen fade
		0	X	OFF
		1	0	fade in
		1	1	fade out
6		reserved		
7		to be cleared		

Table 6: I²C-Register REG6 (ENABLE DIRECT REG. ACCESS): Subaddress 05 hex [00]

Bit	Name	Function
0	SET_HOR_DEL	0: normal mode (HOR_DELAYS=0) 1: HOR_DELAYS value taken from REG12 (direct PROZONIC/ MELZONIC access).
1	SET_HWE	0: normal mode 1: take HWESTA/STO settings from REGs 13, 14
2	SET_HRE	0: normal mode 1: take HRESTA/STO settings from REGs 15, 16
3	SET_HDDEL	0: normal mode 1: take HDDEL setting from REG17
4	SET_HDMSB	0: normal mode 1: take HDMSB setting from REG18
5	SET_VDMSB	0: normal mode 1: take VDMSB setting from REG19
6	SET_HBDA	0: normal mode 1: set HBDASTA/STO ECO values direct via IIC REGs 20, 21
7	SET_HWE_MAIN_ DELAY	0: normal mode 1: HWE main delay via REG 22

Table 7: I²C-Register REG7: Subaddress 06 hex [00]

Bit	Name	Function
0	SET_HBOX	0: default mode 1: direct control of HBOX_START/STOP via IIC REGs 31, 32
1		to be cleared
2		to be clerared
3	SET_VBDA	0: default mode 1: direct VBDASTA/STO via REGs 29, 30
4		to be cleared
5		to be cleared
6	SET_HDAV	0: default 1: direct HDAVSTA/STO control via IIC REGs 25, 26
7		to be cleared

Table 8: I²C-Register REG8 (VWE DELAY): Subaddress 07 hex [00]

Bit	Name	Function
0	VWED0	VWE delay bit 0
1	VWED1	VWE delay bit 1
2	VWED2	VWE delay bit 2
3	VWED3	VWE delay bit 3
4	VWED4	VWE delay bit 4
5	VWED5	VWE delay bit 5
6	VWED6	VWE delay bit 6
7	VWEX	0 = off, normal mode 1 = on, reduced vertical write window shiftable by VWED0...D6

Table 9: I²C-Register REG9 (Test-REG: BLANK FIELDS): Subaddress 08 hex [80]

Bit	Name	Function
0	BLANK_F0	blank field 0
1	BLANK_F1	blank field 1
2	BLANK_F2	blank field 2
3	BLANK_F3	blank field 3
4...7	reserved	

Table 10: I²C-Register REG10: Subaddress 09 hex [00]

Bit	Name	Function
0		to be cleared
1		to be cleared
2		to be cleared
3		to be cleared
4	DIGITAL_COLOR_ DECODER_ CONCEPT	0: Analog color decoder concept 1: Digital color decoder concept (internal acquisition PLL switched off; external clock, 16 MHz line locked expected)
5	CLR_MOVIE	0: default mode 1: clear AUTO_MOVIE flag (forced)
6	NPIP_4x4	0: no 4x4 PIP, take NPIP 1: 4x4 PIP
7		to be cleared

Table 11: I²C-Register REG11 (Port Settings): Subaddress 0A hex [30]

Bit	Name	Function
0	P11	0: clear port pin P1.1 1: set port pin P1.1
1	P12	0: clear port pin P1.2 1: set port pin P1.2
2	P14	0: clear port pin P1.4 1: set port pin P1.4
3	P15	0: clear port pin P1.5 1: set port pin P1.5
4	MELZ_PROZ	Software selection, only valid if SW_HW=1 0: PROZONIC 1: MELZONIC
5	SW_HW	enable the software selection between PROZONIC/MELZONIC 0: Hardware selection via Pin P1.3 1: Software selection with MELZ_PROZ
6	reserved	
7		to be cleared

Table 12: I²C Register REG12 (HOR_DELAYS): Subaddress 0B hex [28]

Bit	Name	Function
0...2	IN_DEL	input luminance delay
3...4	HD_DEL (Prozonic)	1 to 4 clock shift for the hor. reference
	WE_HDEL (Melzonic)	1 to 4 clock shift for WE2 output signal
5...6	WE2_DEL (Prozonic)	1 to 4 clock shift for WE2 output signal
	RE_HDEL (Melzonic)	1 to 4 clock shift for RE output signals
7		reserved

Table 13: I²C Register REG13 (HWESTA): Subaddress 0C hex [xx]

Bit	Name	Function
0 ... 7	HWESTA	start value for horizontal write enable (lower 8 bits)

Table 14: I²C Register REG14 (HWESTO): Subaddress 0D hex [xx]

Bit	Name	Function
0 ... 7	HWESTO	stop value for horizontal write enable (lower 8 bits)

Table 15: I²C Register REG15 (HRESTA): Subaddress 0E hex [1F]

Bit	Name	Function
0 ... 7	HRESTA	start value for horizontal read enable (lower 8 bits)

Table 16: I²C Register REG16 (HRESTO): Subaddress 0F hex [C3]

Bit	Name	Function
0 ... 7	HRESTO	stop value for horizontal read enable (lower 8 bits)

Table 17: I²C Register REG17 (HDDEL): Subaddress 10 hex [00]

Bit	Name	Function
HDDEL: horizontal fine delay for the SAA 4977 display signals		
0	HDAV_DEL	fine delay of HDAV 0: no additional delay 1: signal delayed by one display clock

Table 17: I²C Register REG17 (HDDEL): Subaddress 10 hex [00]

Bit	Name	Function
1	HBDA_DEL	fine delay of HBDA 0: no additional delay 1: signal delayed by one display clock
2	HRE_DEL	fine delay of HRE 0: no additional delay 1: signal delayed by one display clock
3	HBLND_DEL	fine delay of HBLND 0: no additional delay 1: signal delayed by one display clock

Table 18: I²C Register REG18 (HDMSB): Subaddress 11 hex [AA]

Bit	Name	Function
0	HDMSB	MSB of HDAVSTA
1		MSB of HDAVSTO
2		MSB of HBDASTA
3		MSB of HBDASTO
4		MSB of HRESTA
5		MSB of HRESTO
6		MSB of HBLNDSTA
7		MSB of HBLNDSTO

Table 19: I²C Register REG19 (VDMSB): Subaddress 12 hex [0A]

Bit	Name	Function
0	VDMSB	to be cleared
1		to be set
2		MSB of VBDASTA
3		MSB of VBDASTO
4...7		reserved

Table 20: I²C Register REG20 (HBDASTA): Subaddress 13 hex [52]

Bit	Name	Function
0 ... 7	HBDASTA	start value of horizontal blanking for the DAC (lower 8 bits)

Table 21: I²C Register REG21 (HBDASTO): Subaddress 14 hex [F2]

Bit	Name	Function
0 ... 7	HBDASTO	stop value of horizontal blanking for the DAC (lower 8 bits)

Table 22: I²C Register REG22 (HWE MAIN DELAY): Subaddress 15 hex [32]

Bit	Name	Function
0 ... 7	HWE_MAIN_DELAY	horizontal shift of the HWE signal

Table 23: I²C Register REG23 : Subaddress 16 hex [xx]

Bit	Name	Function
0 ... 7	reserved	

Table 24: I²C Register REG24: Subaddress 17 hex [xx]

Bit	Name	Function
0 ... 7	reserved	

Table 25: I²C Register REG25 (HDAVSTA): Subaddress 18 hex [05]

Bit	Name	Function
0 ... 7	HDAVSTA	start value of gating signal for chrominance display data (lower 8 bits)

Table 26: I²C Register REG26 (HDAVSTO): Subaddress 19 hex [A9]

Bit	Name	Function
0 ... 7	HDAVSTO	stop value of gating signal for chrominance display data (lower 8 bits)

Table 27: I²C Register REG27 : Subaddress 1A hex [xx]

Bit	Name	Function
0 ... 7	reserved	

Table 28: I²C Register REG28 : Subaddress 1B hex [xx]

Bit	Name	Function
0 ... 7	reserved	

Table 29: I²C Register REG29 (VBDASTA): Subaddress 1C hex [15]

Bit	Name	Function
0 ... 7	VBDASTA	start value of vertical blanking for the DAC (lower 8 bits)

Table 30: I²C Register REG30 (VBDASTO): Subaddress 1D hex [31]

Bit	Name	Function
0 ... 7	VBDASTO	stop value of vertical blanking for the DAC (lower 8 bits)

Table 31: I²C Register REG31 (HBOX_START): Subaddress 1E hex [00]

Bit	Name	Function
0 ... 7	HBOX_START	direct PROZONIC/MELZONIC register access

Table 32: I²C Register REG32 (HBOX_STOP): Subaddress 1F hex [00]

Bit	Name	Function
0 ... 7	HBOX_STOP	direct PROZONIC/MELZONIC register access

Table 33: I²C Register REG33: Subaddress 20 hex [xx]

Bit	Name	Function
0 ... 7	reserved	

Table 34: I²C Register REG34: Subaddress 21 hex [xx]

Bit	Name	Function
0 ... 7	reserved	

3.2.3 I²C translater register data format

Next subaddress for the following I²C registers will be 28h !

Acquisition part:

Table 35: I²C Translater Register 0 (ACQ_0): Subaddress 28 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	AGC_Y	0150	00	AGC gain for Y channel (2´s complement rel 0 dB): upper 8 bits

Table 36: I²C Translater Register 1 (ACQ_1): Subaddress 29 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	AGC_UV	0151	00	AGC gain for U and V channel (2´s complement rel 0 dB): upper 8 bits

Table 37: I²C Translater Register 2 (ACQ_2): Subaddress 2A hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0	AGC_Y_LSB	0152	00	AGC gain for Y channel LSB
1	AGC_UV_LSB			AGC gain for UV channel LSB
2	standby_f			1: frontend in standby mode
3	aaf_bypass			1: bypass for prefilter
4				reserved
5				reserved
6				reserved
7				reserved

Table 38: I²C Translater Register 3 (ACQ_3): Subaddress 2B hex

Bit	Name	Host address (hex)	Default value (hex)	Function			
0..1	UVclcorrect_mode	0153	00	Bit1	Bit0	UV clamp mode	
				0	0	auto	
				0	1	fixed	
				1	0	keep	
				1	1	-	
2..4	Uclcorrect_fval		000	Bit2	Bit1	Bit0	fixed value clamp corr. U channel
				0	0	0	
				0	0	1	
				0	1	0	
				0	1	1	
				1	0	0	
				1	0	1	
				1	1	0	
				1	1	1	
5..7	Vclcorrect_fval		000	Bit2	Bit1	Bit0	fixed value clamp corr. V channel
				0	0	0	
				0	0	1	
				0	1	0	
				0	1	1	
				1	0	0	
				1	0	1	
				1	1	0	
				1	1	1	

Table 39: I²C Translater Register 4 (ACQ_4): Subaddress 2C hex

Bit	Name	Host address (hex)	Default value (hex)	Function		
0..1	UVcoring	0154	00	Bit1	Bit0	UV coring level
				0	0	0
				0	1	+/- 0,5
				1	0	+/- 1
				1	1	+/- 2
2..3	mff_width		01	Bit1	Bit0	majority filter setting
				0	0	1
				0	1	3
				1	0	5
				1	1	7
4..5	UVcl_tau		00	Bit1	Bit0	vertical filtering of measured clamp
				0	0	
				0	1	
				1	0	
				1	1	
6	compress		0	0: compression off 1: compression on		
7	comp_mode		0	0: 14:9 compression mode 1: 16:9 compression mode		

Table 40: I²C Translater Register 5 (ACQ_5): Subaddress 2D hex

Bit	Name	Host address (hex)	Default value (hex)	Function			
0..2	ydelay	0155	000	Bit2	Bit1	Bit0	variable Y-delay
				0	0	0	-2
				0	0	1	-1
				0	1	0	0
				0	1	1	1
				1	0	0	2
				1	0	1	-
				1	1	0	-
				1	1	1	-
3..4	overl_comp		01	Bit1	Bit0	overload threshold	
				0	0	216	
				0	1	224	
				1	0	232	
				1	1	240	
5	fill_mem			0: default 1: fill memory with constant value			
6				reserved			
7				reserved			

Display part:

Table 41: I²C Translater Register 6 (DCTI_0): Subaddress 2E hex

Bit	Name	Host address (hex)	Default value (hex)	Function			
0..2	dcti_gain	01D1	010	Bit2	Bit1	Bit0	dcti gain
				0	0	0	0
				0	0	1	1
				0	1	0	2
				0	1	1	3
				1	0	0	4
				1	0	1	5
				1	1	0	6
				1	1	1	7
3..6	dcti_threshold		0000	DCTI threshold (0,1,2,...,14,15)			
7	dcti_ddx_sel		1	DCTI ddx_sel 0: low 1: high			

Table 42: I²C Translater Register 7 (DCTI_1): Subaddress 2F hex

Bit	Name	Host address (hex)	Default value (hex)	Function		
0..1	dcti limit	01D2	10	Bit1	Bit0	DCTI limit
				0	0	0
				0	1	1
				1	0	2
				1	1	3
2	dcti_separate		1	0: off 1: on		

Table 42: I²C Translater Register 7 (DCTI_1): Subaddress 2F hex

Bit	Name	Host address (hex)	Default value (hex)	Function
3	dcti_protection		1	0: off 1: on
4	dcti_filteron		1	0: off 1: on
5	dcti_superhill		1	0: off 1: on
6...7	nrln_0		00	DCTI number lines (2 LSBs)

Table 43: I²C Translater Register 8 (DCTI_2): Subaddress 30 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	nrln_1	01D3	0FF	DCTI number lines upper 8 bits

Table 44: I²C Translater Register 9 (DCTI_3): Subaddress 31 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	nrpx	01D4	0D8	DCTI number of pixels / 4

Table 45: I²C Translater Register 10 (SIDEP_OVL_UV): Subaddress 32 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 3	overlay_u	01D5	1000	sidepanels overlay U 4 MSB
4 ... 7	overlay_v		1000	sidepanels overlay V 4 MSB

Table 46: I²C Translater Register 11 (SIDEP_OVL_Y): Subaddress 33 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	overlay_y	01D6	00	sidepanels overlay Y 8 MSB

Table 47: I²C Translater Register 12 (PEAKING): Subaddress 34 hex *)

Bit	Name	Host address (hex)	Default value (hex)	Function		
0..1	peak_a	01D7	10	Bit1	Bit0	peaking a
				0	0	0
				0	1	1/2
				1	0	1
				1	1	2
2..3	peak_b		10	Bit1	Bit0	peaking b
				0	0	0
				0	1	1/2
				1	0	1
				1	1	2
4..5	peak_limit		10	Bit1	Bit0	peak limiter setting
				0	0	255
				0	1	340
				1	0	425
				1	1	511
6..7	peak_coring		10	Bit1	Bit0	peak coring settings
				0	0	0
				0	1	4
				1	0	8
				1	1	16

The peaking function will be improved in the next SAA 4977 version.

Table 48: I²C Translater Register 13 (SIDEP_START) Subaddress 35 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	sidepanel_start	01D8	00	sidepanel start position (8 MSB)

Table 49: I²C Translater Register 14 (SIDEP_STOP): Subaddress 36 hex

Bit	Name	Host address (hex)	Default value (hex)	Function
0 ... 7	sidepanel_stop	01D9	00	sidepanels stop position (8 MSB)

Table 50: I²C Translater Register 15 (SIDEP_FDEL): Subaddress 37 hex *)

Bit	Name	Host address (hex)	Default value (hex)	Function		
0...1	sidepanel_fdel	01DAh	00	Bit1	Bit0	sidepanel fine delay
				0	0	0
				0	1	1
				1	0	2
				1	1	3
2	display_mode		0	display mode 0: 9 bit, blanking level 288 1: 10 bit, blanking level 64		
3				reserved		
4				reserved		
5				reserved		
6				reserved		
7				reserved		

*) The IIC register, subaddress 37 can only be controlled in the Melzonic mode (subaddress 0A hex, bit 4, MELZ_PROZ = 1)

3.2.4 Acknowledgement of bytes

The IPQ µC acknowledges always all register bytes independent from their contents. If the master µC transmits more than the maximum number of register bytes, the slave µC will acknowledge the following bytes, but will not store them in its internal RAM.

3.3 Receiving data from the IPQ µC

The IPQ µC is able to transmit one status byte plus additional read bytes to the main µC. The IPQ µC then works as a slave transmitter.

The I²C-bus transmission protocol for transmitting the status byte plus read registers has the following format:

Start	Slave address 69h	Ack	Status byte	ReadReg1	Ack	...	Nack	Stop

3.3.1 Contents of status byte

The status byte contains the following information:

Table 51: I²C Read Register 1 (STATUS): No Subaddress !

Bit	Name	Default value (hex)	Function
0	NON_IL	0	0: non interlaced mode not active 1: non interlaced mode active
1			reserved
2	AUTO_MOVIE_FLAG	0	0: normal mode 1: automatic movie mode activated
4	MOVIE		0: no movie mode detected 1: movie detected
4	PHASE_FLAG	0	0: standard mode (ABAB in case of MOVIE=1) 1: 180° phase shift (BCBC, MOVIE=1)
5	PORT	0	bit setting read from port bit P2.4 0: P2.4 = 0 1: P2.4 = 1
6	READY	1	0: not ready to accept command 1: ready to accept command
7	WATCH	0	Watchdog bit: will be toggled when status byte is read by master µC, initialized with 0

Bit 6 will be cleared after the IPQ µC has received I²C register bytes. It will be set again after the evaluation of all bytes is completed and an external interrupt (V100) initiating data transfer from IPQ µC to ECO5, datapath additional registers, PROZONIC/MELZONIC is not currently serviced.

3.3.2 Contents of datapath read registers

Table 52: I²C Read Register 2 (MPD MSByte1): No Subaddress !

Bit	Name	Function
0...7	MOVIE_PHASE_A	direct PROZONIC register read, MSByte; Movie phase detection byte 1

Table 53: I²C Read Register 3 (MPD MSByte2): No Subaddress !

Bit	Name	Function
0...7	MOVIE_PHASE_B	direct PROZONIC register read, MSByte; Movie phase detection byte 2

Table 54: I²C Read Register 4 (read_Uclerror): No Subaddress !

Bit	Name	Host address (hex)	Function (NOT YET IMPLEMENTED !!!)
0...6	read_Uclerror	0170	Read U channel clamp error (+3/-4 resolution 1/16 LSB)
7			reserved

Table 55: I²C Read Register 5 (read_Vclerror): No Subaddress !

Bit	Name	Host address (hex)	Function (NOT YET IMPLEMENTED !!!)
0...6	read_Vclerror	0171	Read V channel clamp error (+3/-4 resolution 1/16 LSB)

Table 55: I²C Read Register 5 (read_Vclerror): No Subaddress !

Bit	Name	Host address (hex)	Function (NOT YET IMPLEMENTED !!!)
7			reserved

Table 56: I²C Read Register 6 (read_Ygain): No Subaddress !

Bit	Name	Host address (hex)	Function (NOT YET IMPLEMENTED !!!)
0...7	read_Ygain	0172	Read overflow indication of Y channel

Table 57: I²C Read Register 7 (AGC_Y_read): No Subaddress !

Bit	Name	Host address (hex)	Function (NOT YET IMPLEMENTED !!!)
0...7	AGC_Y_read	0173	AGC gain for Y channel, upper 8 bits (for functional test only)

3.4 Timing aspects

The maximum allowed response time between accepting register bytes and the execution of the commands handled by the IPQ µC is 90 ms. This time is only relevant when field memory control modes are changed. Field memory control modes are: Cine, LFR, Still, Multi-PIP mode. When a field memory control mode has been activated, the IPQ µC waits max. 40 ms until a new frame starts in LFR mode (4 x 100Hz field repetition time). Then it takes another 40 ms until one new frame has been completely transmitted in order to run the new mode.

The maximum allowed total clock stretch time of the IPQ µC within one I²C message is 5 ms.

The minimum wait time between sending two I²C bus register data packages varies from 12 ms (no field memory control modes have changed) to 90 ms (field memory control modes have changed).

If the user wants to make sure that a complete I²C bus register data package is transmitted without being interrupted by VDFL IRQ µC routine and the slave µC is free for I²C after the master µC transmits I²C data, the I²C data package should be transmitted between 3 and 5 ms after VDFL occured. The slave µC sets bit 6 of the status byte when it is ready to accept I²C commands.

Multi-PIP:

The time between one live PIP picture register command to another should not be shorter than 120 ms.

Screen fade:

As long as this mode is active (86 fields = 860 ms in normal mode), all other mode changes are ignored.

4. Evaluation of I²C-bus register data

The evaluation of I²C bus register data is done with respect to a certain priority structure. In the following sections certain restrictions on bit settings in the I²C register bytes which limit the possibilities of combining field memory control modes (Cine, LFR, Still, Multi-PIP mode) and/or secondary control commands are listed.

There are 3 different application concepts for BESIC, which are taken into account:

1. MELZONIC concept:

- two field memory concept with Natural Motion (Movement Estimation and Compensation), LFR, Adaptive NR, External Multi PIP

2. PROZONIC concept:

- two field memory concept with LFR, Adaptive NR, External Multi PIP

3. Single memory concept:

- simple AABB processing

All functions which are related to only one or two of the 3 concepts, are indicated.

4.1 Field memory control modes

4.1.1 Priorities

The different Field Control Modes of the IPQ module have different priorities. The following table shows which mode has the highest and which mode has the lowest priority. The priority structure must be taken into account when activating field control modes.

Table 58 Mode Priorities

Mode	Priority
INIT	highest
SCREEN FADE (not yet implemented)	.
MPIP	.
VZOOM	
GENERATOR mode	.
FEATURE mode	.
NON_IL mode	.
Natural Motion (MELZONIC concept)	.
LFR mode (MELZONIC/PROZONIC concept)	.
AABB mode	lowest

4.1.2 Field Control modes

AABB Mode

Software control: Mode with the lowest priority (all other field control bits switched off).

The AABB mode is the most simple conversion mode for 100 Hz. Only one field memory is implemented. The video data of an incoming field are simply doubled in an AABB sequence. For the low-end concept this mode is the default conversion mode.

This mode can also be used in the PROZONIC and MELZONIC concept. The mode even has to work correctly if the PROZONIC and MELZONIC is removed. This demand means that the vertical display read control has to be realized via the memory controller part of SAA 4977 and not by the VRE control of the external processing ICs. In the live AABB mode the DR-Bit has to be toggled field by field to generate the AABB raster with the field length sequence 313, 312.5, 312 and 312.5 lines.

LFR Mode

Software Control: I²C-Register subaddress 01, Bit 0 (LFR)

The Line Flicker Reduction (LFR) mode is the default control mode of the PROZONIC concept and can be used with MELZONIC as well. It makes use of a medianfilter to generate the output sequence: original field A, medianfiltered A*, medianfiltered B* and original field B.

Natural Motion (Video and Movie)

Software Control: I²C-Register subaddress 02, Bit 4 (NATURAL_MOTION)

This function can only be realized in the high-end Melzonic concept. The MELZONIC will compensate movement artefacts which are caused by e.g. simple field doubling in the

100 Hz mode. For video sources with 50 Hz motion resolution a constant 100 Hz motion is calculated by a vector based motion estimation and compensation. For movie sources which have a motion resolution of only 25 Hz the MELZONIC is able to increase the motion frequency to 50 Hz. This provides a remarkable improvement for the display of movies even compared to 50 Hz standard TVs. A recursive block matching algorithm is implemented in the SAA 4991. Beside the simple field control of these two natural motion modes the software has to check the quality of the motion compensation. The µC in the SAA 4977 reads the MELZONIC register NR_BAD_RANGES. This register will be compared with the constant threshold value BAD_LIMIT. If NR_BAD_RANGES is greater than BAD_LIMIT the Natural Motion Mode will be disabled, even if the I²C-bus bit NATURAL_MOTION equals 1. The 100 Hz conversion mode will be switched into the mode, which would have been chosen if NATURAL_MOTION is cleared (fallback mode). It is a control mode with a lower priority, in which no vector based processing is performed.

As mentioned above the natural motion processing has to be adapted to the motion resolution of the source. For this requirement it is necessary to detect if a movie or a video source has to be motion compensated. The correct mode (video or movie processing) can be controlled by the user himself or by an automatic routine (see AUTO_MOVIE).

ABAB Movie Mode

Software Control: I²C-Register subaddress 01, Bit 4 (MOVIE), NATURAL_MOTION cleared

This mode is supported by the PROZONIC and MELZONIC approach. The converter performs a frame repetition. The phase relation between the movie pictures and the incoming video signal is not standardized. Via the additional control bit PHASE (I²C-Register subaddress 01, bit 5) the processing is put into the correct phase relation to the incoming movie (ABAB or BCBC).

Satellite Mode

Software Control: I²C-Register subaddress 02, Bit 6 (SAT_MODE)

In the satellite mode all the four 100 Hz display fields are derived from the output of the median filter. The median filter will filter out details occurring in only one line. This fact can be used to attenuate typical FM noise dropouts which normally occur uncorrelated in the field. A bad satellite signal reception can be improved quite effectively in this mode without deteriorating the picture quality.

Generator Mode (G_Mode)

Software Control: I²C-Register subaddress 00, Bit 2(G_MODE)

The bit G_MODE activates a stable 100 Hz display with a fixed field length of 312.5 lines for AFF=0 and 262.5 lines for AFF=1. The display field length is not adapted according to the video source. The conversion mode is reduced to a single field repetition mode (AAAA). This special mode can be used to get a stable OSD picture without a source or with a very noisy source. It does also improve the picture stability for a tuner channel search.

Auto Movie Detection routine

Software Control: I²C-Register subaddress 01, Bit 6 (AUTO_MOVIE)

- Auto Movie Detection in the Melzonic concept

The bit AUTO_MOVIE activates an automatic movie source detection if the natural motion mode is switched on. The detection is based on the read values of the Melzonic registers “vector_sum”. This sum of vector absolutes represents the amount of motion found between two incoming fields. The software investigates the vector sums of a whole frame to detect whether a video or a movie source is connected. If the two values show a large difference the converter can be switched to a vector based movie processing increasing the movement resolution from 25 Hz to 50 Hz. The annoying motion judder of movies is eliminated. The phase relation between the movie pictures and the video fields is taken into account. In case of a video source or scenes with no or small motion the video processing is active, increasing the movement resolution from 50 Hz to 100 Hz. This removes the unsharpness of moving edges compared to a simple field repetition 100 Hz converter.

If the AUTO_MOVIE bit is set to zero, the converter is performing a motion compensation processing for video sources as long as the bit MOVIE is cleared. If MOVIE is set a movie motion compensation is activated. The phase relation to the incoming movie can be adapted via the control bit MOVIE_PHASE. The user is able to adapt the natural motion processing to the source via the bits MOVIE and MOVIE_PHASE by himself if the automatic movie detection routine has been switched off.

- Auto Movie Detection in the Prozonic concept (not implemented in the SAA 4977 V1B)

If the bit AUTO_MOVIE is set in the Prozonic concept the same routine as descibed above will investigate whether a movie source is applied and in which phase relation it is transmitted. The software uses the Prozonic read register MPD to get a motion information which is not based on a vector sum but on a sum of absolute differences in the luminance channel. With Prozonic the movie detection is not used to activate a movie mode. The LFR sequence AA*B*B is adapted to the phase of a movie and can be switched to a BB*C*C processing automatically. This results in an improved performance of vertical rolling titles. The time constant of the Auto Movie routine is increased compared to the Melzonic approach. There is no need for a fast detection because no severe artefacts occur if the detection has a delay.

Multi-PIP (MPIP)

Software Control: I²C-Register subaddress 03, Bit 6 (MPIP)

The field memories of the 100 Hz converter can be used to generate a MPIP picture if MPIP is set. It is assumed that the TV set contains a PIP Module which generates a compressed PIP picture at the bottom right side of the screen. The picture supplied by the PIP module is written into the field memories and placed according to the chosen position of the MPIP control (I²C-Register subaddress 03, POS0-POS3). The complete MPIP picture shows 3 x 3 or 4 x 3 small pictures. One of those can display a live source, the others are frozen. With the control bit SPIP (I²C register subaddress 03, bit 7) the PIP window can be adapted to a 60 Hz PIP source. The vertical size of the PIP window is reduced if SPIP is set.The MPIP feature makes use of the boxing function of Prozonic or Melzonic. The noise reduction circuitry (k-factor control) together with the defined boxes support the PIP function. The MPIP feature can be used for a channel overview or to show frozen motion phases of one channel (photo finish).

Vertical Zoom

Software Control: I²C-Register subaddress 02 (VZOOM_0 to VZOOM_3, bit 0 to bit 3 and VZOOM, bit 7)

A vertical zoom function realized by an interpolation of lines can be activated via the control bit VZOOM. The zoom factor is defined by the bits VZOOM_0 to VZOOM_3. The factors 1.1, 1.25, 1.33 and 1.5 are supported by the control software. The zoom function can be combined with the LFR and the natural motion feature (video and movie source). If the AABB mode is chosen together with vertical zoom the software switches automatically to a LFR processing.

Still Picture Mode

Software Control I²C Register subaddress 01, bit 7(STP)

The Still Picture function can be combined with every conversion mode. For the modes LFR and Natural Motion the frozen picture is processed based on a frame displaying the original field A and the median filtered A*. In the AABB mode, MPIP, SAT Mode and Generator Mode only a one field still picture is generated.

Non-Interlace Mode

Software Control: no I²C control

If a non-interlace source is detected by the software the field processing switches automatically into a Non-Interlace Mode. The detection criteria is a field length which is N complete lines. As the memory controller counts half lines starting with zero a non-interlace source will set the LSB of the field length read register (PAL standard = 270 hex, NTSC standard = 20C hex). A non-interlace source is additionally indicated in bit 0 of the status read register 1 (NON_IL).

INIT

Software Control I²C Register subaddress 0, bit 7 (INIT)

If the Init bit is set the SAA 4977 module will be initialized with the default values.

The module is initialized in the Melzonic concept in the natural motion mode with AUTO_MOVIE=1. Furthermore the SAA 4977 is initialized in the digital colour deccoder mode. For this reason the picture will appear disturbed in the analog concept after an initialization has been done.

4.1.3 Secondary control commands

The secondary control commands can be combined with the above described field control modes

Acquisition Field Frequency selection (AFF)

Software Control I²C Register subaddress 0, bit 4(AFF)

The bit AFF is set by the user according to the vertical frequency of the incoming source. In case of a 50 Hz source the bit is cleared, for 60 Hz sources it is set. The vertical writing window is adapted (VWE1STA and VWE1STO). The bit also changes the reference field length for the feature mode detection. In the generator mode the field length is set to 312.5 lines for AFF=0 and 262.5 lines for AFF=1.

Horizontal Compression

Software Control: not yet directly supported

The SAA 4977 supports two different compression modes for 14:9 and 16:9 display modes (1.17 and 1.33). These modes can be activated via the datapath register subaddress 2C, bits 6 and 7. Additionally a correct setting of the horizontal memory controller settings has to be done (see control table in chapter 5)

Noise reduction

Software Control: I²C-Register, subaddress 04, bit 0 and 1 (NR0, NR1)

The recursive noise reduction can be set to three levels (low, medium, high). For investigation purposes a direct control of the PROZONIC/MELZONIC noise reduction registers is possible.

Split Screen

Software Control: I²C-Register subaddress 04, Bits 2, 3 (SPS0, SPS1)

The screen can be split into two halves by the Split Screen feature. One half is showing a noise reduced picture the other the performance of the original source. The splitting can be done in horizontal or vertical direction. The mode allows a direct comparison of the original and noise reduced picture on the screen.

Screen fade

Software Control: I²C-Register subaddress 04, Bit 4, 5 (SCF0, SCF1)

The screen fade feature can be used to “fade out” a picture like closing curtains. This is done by the control SW by continuously changing the setting of the side panel start and stop values of SAA 4977 until a homogenous coloured picture is visible. The function is also available the other way round where the picture is “faded in” starting from a complete the display.

HWE Delay

Software Control: I²C-Register subaddress 05, bit 7 (SET_HWE_MAIN_DELAY), subaddress 15 Hex (HWE_MAIN_DELAY)

The horizontal writing window can be delayed via the I²C register HWE_MAIN_DELAY if the control bit SET_HWE_MAIN_DELAY is set.

VWE Delay

Software Control: I²C-Register subaddress 07,bits VWE1D0 - VWE1D6 and VWEX

The vertical writing window can be delayed in steps of lines via the I²C register VWE Delay register if the bit VWEX is set. The possible delay range is 0 to127 lines. The delay function is needed to centre a vertical zoomed picture.

Blank Field Mode

Software Control: I²C-Register subaddress 08, bits 0-3, (BLANK_F0 - BLANK_F3)

The Blank Field Mode allows the user to define which fields of the sequence of the 100 Hz display fields are displayed or blanked. If all the four control bits are cleared the normal active display appears. If one bit is set the corresponding display field will be blanked.

In the AABB mode a blanking of every second field generates a display which is similar to a normal 50 Hz screen. The elimination of the large area flicker can be demonstrated by switching from this mode to a normal 100 Hz display. The blank field mode is normally used for testing purposes.

Selection of the Colour Decoder Concept

Software Control: I²C-Register subaddress 09, bit 4 (DIGITAL_COLOR_DECODER_CONCEPT)

Normally the SAA 4977 is implemented in a concept with an analog colour decoder. In this case the acquisition clock is generated by the SAA 4977 and the internal ADC is used. If the control bit (Digital_ Colour_Decoder_Concept) is set the acquisition clock has to be supplied from external. The digital data are directly fed into the first field memory. From the point of software control all horizontal acquisition register values have to be divided by the factor two. The analog frontend part of SAA 4977 V1B should to be switched into the stand-by mode.

Port Pin Control

Software Control: I²C-Register subaddress 0A hex, bit 0 - bit 3

The free port pins of the µ-Controller core in the SAA 4977 can be controlled via I²C bus. The polarity of the port pins is switched synchronized to VDFL this means synchronized to the display. The port pins P1.1, P1.2, P1.4 and P1.5 can be controlled.

Direct control of the PROZONIC/MELZONIC register HOR_DEL

Software Control: I²C-Register subaddress 05, bit 0 (SET_ HOR_DEL)

If the control bit SET_HOR_DEL is set a direct control of the PROZONIC/MELZONIC register HOR_DELAY is enabled (see Prozonic/Melzonic data sheet) via the I²C register subaddress 0B hex. This register allows a fine delay of the Prozonic/Melzonic memory control output signals with clock accuracy. It further more allows an adjustment of the chrominance reformatting for a correct internal chroma processing. The correct setup should be checked with noise reduction switched on.

Direct control of the PROZONIC/MELZONIC register HBOX_START/STOP

Software Control: I²C-Register subaddress 06, bit 0 (SET_ HBOX)

If the control bit SET_HBOX is set a direct control of the PROZONIC/MELZONIC registers HBOXSTART and HBOXSTOP is enabled (see Prozonic/Melzonic data sheet) via the I²C registers subaddress 1E and 1F hex. The box settings are used for the split screen function and Multi PIP.

Direct change of the memory controller settings in the SAA 4977

Via enable bits the most important signals of the memory controller can be defined by the user. This allows a very flexible use of the SAA 4977 also for changed conditions in the application. Many signals are 9 bit values. If one signal is switched to a direct user control the corresponding I²C registers for the signal start and stop values are enabled. These registers define the lower 8 bit of the complete 9 bit values. The MSBs are defined via an additional MSB register which has to be enabled if necessary.

DAC blanking control

Software Control: I²C-Register subaddress 06, bit 3 (SET_VBDA), subaddress 05, bit 6 (SET_HBDA)

The bit SET_VBDA enables the direct control of the vertical blanking time for the DAC of the SAA 4977 via the I²C registers subaddress 1C hex (VBDASTA, start value) and subaddress 1D hex (VBDASTO, stop value). The sensible programming range of VBDA depends on the field length of the source (PAL 0 to 138 hex, NTSC 0 to 106 hex). If the programmed values are higher than the number of lines of the source (VCR fast forward) the memory controller stops the signal automatically.

The horizontal signal part of the blanking can be controlled in the same way. The bit SET_HBDA enables the direct control of the horizontal blanking time for the DAC via the I²C registers subaddress 13 hex (HBDASTA, start value) and subaddress 14 hex (HBDASTO, stop value). The programming range of HBDA is 0 to 1FF hex. The programming step width is two display clocks. The signal refers to the rising edge of the HDFL signal.

The MSBs of the start and stop values are controlled via additional MSB registers (see chapter MSB control). Normally the user does not have to change the MSB settings as long as small changes are done compared to the default settings.

HWE control

Software Control: I²C-Register subaddress 05 hex, bit 1 (SET_HWE)

If the control bit SET_HWE is set a direct control of the horizontal write enable signal fed to to the first field memory is enabled. The start value is defined via I²C register subaddress 0C hex (HWESTA). The stop value is defined via I²C register subaddress 0D hex (HWESTO). The HWESTA/STO values are 9 bit values. Only the lower 8 bits can be changed by the user. The programming steps have 2 clock accuracy of the acquisition clock. The signal refers to the rising edge of the horizontal reference to the SAA 4977 (HA, pin 22).

HRE control

Software Control: I²C-Register subaddress 05 hex, bit 2 (SET_HRE)

If the control bit SET_HRE is set a direct control of the horizontal read enable signal fed to PROZONIC, MELZONIC or to the first field memory in the single field concept is enabled. The start value is defined via I²C register subaddress 0E hex (HRESTA). The stop value is defined via I²C register subaddress 0F hex (HRESTO). The MSBs are controlled via the IIC register HDMSB (see chapter MSB control).

HDAV control

Software Control: I²C-Register subaddress 06 hex, bit 6 (SET_HDAV)

The control bit SET_HDAV enables the direct control of the horizontal display signal HDAV (Horizontal Data Valid Chrominance). The signal gates the chrominance display signals. A wrong setting results in a partly uncoulored picture. The start value is defined via I²C register subaddress 18 hex (HDAVSTA). The stop value is defined via I²C register subaddress 19 hex (HDAVSTO). The signal refers to the rising edge of HRDFL.

HDDEL control

Software Control: I²C-Register subaddress 05 hex, bit 3 (SET_HDDEL)

A direct control of the memory controller register HDDEL via I²C register subaddress 10 hex is enabled if the control bit SET_HDDEL is set. The register HDDEL defines a fine delay of the horizontal output signals of the SAA 4977 with display clock accuracy. The delay adjustment may be necessary for changes in the concept to ensure a correct processing of the colour difference signals which are coded in a serial format (4:1:1). Every signal can be shifted by one clock or none.

HDMSB control

Software Control: I²C-Register subaddress 05 hex, bit 4 (SET_HDMSB)

If the bit SET_HDMSB is set the memory controller register HDMSB can be directly controlled via IIC bus subaddress 11 hex. It contains the MSBs of the start and stop values of the display related horizontal control signals. The detailes definition of the register bits is described in the IIC table.

VDMSB control

Software Control: I²C-Register subaddress 05 hex, bit 5 (SET_VDMSB)

If the bit SET_VDMSB is set the memory controller register VDMSB can be directly controlled via IIC bus subaddress 12 hex. It contains the MSBs of the start and stop values of the display related vertical control signals. The detailes definition of the register bits is described in the IIC table.

4.1.4 Selection of the Hardware configuration

Software Control: I²C-Register subaddress 0A hex, bit 4 (MELZ_PROZ), bit5 (SW_HW)

The hardware configuration is selected via the port pin P1.3 if the control bit SW_HW is cleared. In case P1.3 is on low level the Prozonic and single field concept is chosen. If P1.3 is on high level the Melzonic concept is active.

If the control bit SW_HW is set the concept is determined by the control bit MELZ_PROZ. For MELZ_PROZ cleared the Prozonic and single field concept is chosen. If MELZ_PROZ is set the Melzonic concept is active.

4.1.5 Datapath translator registers

Software Control: I²C-Register subaddress 30 - 3F hex

Via the I²C registers with subaddress 30 to 3F hex the SAA 4977 datapath registers can be directly accessed. The datapath registers are initialized after power-on but not changed by any other routines than the I²C bus.

For a detailed functional description of the datapath please refer to the application notes AN97057 and AN97071.

4.1.6 SNERT interface

Via the SNERT interface all register data for PROZONIC, MELZONIC or LIMERIC dependant on the chosen hardware configuration is transmitted. The internal SNERT pins of the µC Core of the SAA4977 are directly connected to the pins of the SAA4977 V1C.

5. Default IIC control settings

Table 59: Default IIC settings

IIC reg. subaddr. (hex)	Single field concept			Prozonic concept			Melzonic concept		
	standard	comp. 1.10	comp. 1.33	standard	comp. 1.10	comp. 1.33	standard	comp. 1.10	comp. 1.33
00	00	00	00	00	00	00	00	00	00
01	00	00	00	01	01	01	41	41	41
02	00	00	00	00	00	00	10	10	10
03	00	00	00	00	00	00	00	00	00
04	00	00	00	01	01	01	01	01	01
05	C4	C6	C4	CD	CF	CD	CD	CF	CD
06	40	40	40	40	40	40	40	40	40
07	00	00	00	00	00	00	00	00	00
08	00	00	00	00	00	00	00	00	00
09	00	00	00	00	00	00	00	00	00
0A	20	20	20	20	20	20	30	30	30
0B	00	00	00	A0	A0	A0	28	28	28
0C	00	02	00	00	02	00	00	02	00
0D	00	A5	00	00	A5	00	00	A5	00
0E	3B	53	6D	21	39	51	15	31	49
0F	DF	C0	AD	C5	A6	91	B9	9E	89
10	00	00	00	04	04	04	00	00	00
11	00	00	00	00	00	00	00	00	00
12	00	00	00	00	00	00	00	00	00
13	57	57	57	57	57	57	57	57	57
14	F4	F4	F4	F4	F4	F4	F4	F4	F4
15	26	26	26	27	26	26	27	26	26
16	00	00	00	00	00	00	00	00	00
17	00	00	00	00	00	00	00	00	00
18	21	21	21	21	21	21	21	21	21

Table 59: Default IIC settings

IIC reg. subaddr. (hex)	Single field concept			Prozonic concept			Melzonic concept		
	standard	comp. 1.10	comp. 1.33	standard	comp. 1.10	comp. 1.33	standard	comp. 1.10	comp. 1.33
19	E0	E0	E0	E0	E0	E0	E0	E0	E0
1A	00	00	00	00	00	00	00	00	00
1B	00	00	00	00	00	00	00	00	00
1C	00	00	00	00	00	00	00	00	00
1D	00	00	00	00	00	00	00	00	00
1E	00	00	00	00	00	00	00	00	00
1F	00	00	00	00	00	00	00	00	00
20	00	00	00	00	00	00	00	00	00
21	00	00	00	00	00	00	00	00	00
28	00	00	00	00	00	00	00	00	00
29	00	00	00	00	00	00	00	00	00
2A	00	00	00	00	00	00	00	00	00
2B	00	00	00	00	00	00	00	00	00
2C	04	44	C4	04	44	C4	04	44	C4
2D	08	08	08	08	08	08	08	08	08
2E	82	82	82	82	82	82	82	82	82
2F	32	32	32	32	32	32	32	32	32
30	FF	FF	FF	FF	FF	FF	FF	FF	FF
31	D8	D8	D8	D8	D8	D8	D8	D8	D8
32	88	7A	7A	88	7A	7A	88	7A	7A
33	00	4D	4D	00	4D	4D	00	4D	4D
34	AA	AA	AA	AA	AA	AA	AA	AA	AA
35	00	EA	E2	00	E8	E0	00	EB	DF
36	00	3C	4A	00	3B	47	00	3E	48
37	-	-	-	-	-	-	00	00	00

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